Design of the 10-MHz IF Amplifier for the Block IV Subcarrier Demodulator Assembly

P. F. Kuhnle
R.F. Systems Development Section

The design effort was started in September 1971 to design and build the Block IV subcarrier demodulator assembly (SDA). The design goals were (1) remote control of the adjustable parameters (gain and bandwidth) to allow automatic calibration and control; (2) increased package density to reduce cabinet space over the Block III SDA and improve performance at high symbol rates; and (3) improved linear dynamic range and extended symbol rate range. This article will review the basic design and current status.

I. Introduction

The Block IV subcarrier demodulator assembly is scheduled for implementation into the DSN during the first quarter of FY'75.

The following design criteria for the 10-MHz intermediate frequency (IF) amplifier assemblies will be reviewed in this article:

(1) Required design specifications

(2) Block diagram of the 10-MHz intermediate frequency (and video) amplifier assemblies

(3) Signal and noise profile

(4) Hardware improvements over Block III SDA

(5) Current status

For a basic overall Block IV SDA design background, see Ref. 1.

II. Design Specifications

The specifications applicable to determine the IF amplifier design are shown in Table 1. These were based on a review of future missions and on previous development work on the Block III SDA.

III. Block Diagram

The block diagram of the data channel is shown in Fig. 1. This discussion will be limited to the 10-MHz channel located in the quadrature generator assembly, the selectable bandwidth filter assembly, and the 10-MHz section of the coherent amplitude detector assembly. These assemblies are standard Block IV radio frequency (RF) modules, interchangeable without operator adjustment to that module.

Controls are divided into three categories: (1) factory alignment, (2) SDA calibration, and (3) internal pro-

grammable gain and bandwidth switching. All factory alignment controls are entirely contained within the assembly and are not available to operating personnel.

The programmable calibration controls consist of two continuously adjustable analog-controlled attenuators. The quadrature channel gain balance is used to correct the gain error between the data and quadrature channels. The receiver (RCV) 1 or 2 gain control is used to correct the overall gain error between the receiver and SDA.

The gain and bandwidth switching is controlled digitally in several discrete ranges, depending on the desired symbol rate. The gain switching before and after the quadrature generator phase switch is designed in several steps, with the resultant overall gain for all steps being constant. Gain switching was required to reduce the subcarrier leakage through the phase switch. This leakage is caused by imperfections in the mixer which allow the subcarrier frequency harmonics to pass through the IF amplifier as an added signal to the expected products. The leakage becomes increasingly pronounced in the wider bandwidths at high symbol rates because the channel cannot discriminate against the unwanted subcarrier and yet pass the desired data stream.

To reduce this leakage, the gain for each gain/bandwidth step, before the subcarrier phase switch, was increased to the maximum permissible that would still maintain the design point signal-to-noise linearity. The gain, after subcarrier demodulation, is programmed to maintain constant overall IF amplifier gain.

Post-subcarrier demodulation bandwidth switching was utilized to retain the design point signal-to-noise ratio linearity of the RF amplifiers, double-balanced mixers, and video amplifiers.

It is necessary to maintain a constant 10-MHz phase shift for all the multiple gain/bandwidth steps. Phase shift due to gain switching with solid state attenuators was not a problem. Bandwidth switching required the insertion of the several bandpass filters into the amplifier. It was not economical to procure filters with the identical phase shift for all multiple steps. To correct these phase errors in the signal path, a preset factory adjustable phase shifter was inserted in the 10-MHz reference path. This was accomplished by designing a continuously adjustable, voltage-variable phase shifter programmed for the required phase shift to compensate the phase errors in the signal path. The phase shifter is located in the selectable bandwidth filter assembly, along with the multiple bandwidth filters, to preserve the module interchangeability concept.

IV. Signal and Noise Profile

The signal-to-noise power ratio, in the particular IF bandwidth, vs. symbol rate for the after subcarrier demodulation is shown in Fig. 2.

Six programmable filter bandwidths were chosen to cover the symbol rate range from 8.33 to 500K symbols per second (SPS). A margin of 7 dB minimum has been allowed between the RMS noise power and the IF amplifier 1-dB gain compression level. Gain switching is coincident with the switching of the six filter bandwidths. Two continuously variable 0- to 20-dB RF attenuators are located ahead of the subcarrier demodulator phase switch. It is necessary to maintain the maximum design point signal plus noise power into the quadrature generator to reduce the subcarrier leakage into the IF amplifier. Two additional continuously variable 0- to 20-dB RF attenuators are located after the subcarrier demodulator phase switch. These act as complementary attenuators to maintain constant gain for the complete IF amplifier channel. The signal and noise levels (referred to in Fig. 1) for the six gain/bandwidths are presented in Table 2. The noise levels shown are at the design point for the minimum symbol rate in each bandwidth.

V. Hardware Improvements

Hardware improvements in the IF amplifier (compared to the Block III SDA) include the use of wideband integrated-circuit amplifiers, solid-state RF attenuators, high-level double-balanced mixers, and greater-density packaging concepts.

The wideband RF amplifier series selection was based on (1) gain and phase-shift characteristics at 10 MHz, (2) the fact that various model amplifiers in the series could be cascaded to increase the dynamic range upper limit, and (3) the use of the same amplifier package on all applications to allow efficient design.

Solid-state RF attenuators were used in place of mechanically switched attenuators. Each attenuator is continuously adjustable and set during factory alignment with a series of potentiometers multiplexed for each programmable gain step.

The double-balanced mixers have a 10-dB greater dynamic range and lower intermodulation distortion than

units available several years ago. Each of the three module types is packaged in one of the new DSN RF modules. This high-density packaging reduces the space required to contain the same generic hardware used in the Block III SDA, thus decreasing the delay time between circuits and permitting the use of higher symbol rates.

VI. Current Status

The engineering models for the modules shown in Fig. 1 have been assembled. Initial in-process tests have indicated that the specifications in Table 1 will be met. A future report will cover the final results.

Reference

1. Crow, R. B., "Block IV Subcarrier Demodulator Assembly Design," in *The Deep Space Network*, Technical Report 32-1526, Vol. XVI, Jet Propulsion Laboratory, Pasadena, Calif., Aug. 15, 1973.

Table 1. Design specifications for Block IV SDA

Parameter	Specification[a]
Symbol rate	8.33 to 500K SPS
Subcarrier frequency range	100 Hz to 1 MHz
IF center frequency	10 MHz
Input bandwidth (prior to subcarrier demodulation)	7 MHz min. at −1 dB 11 ±1 MHz at −3 dB
Data bandwidth (after subcarrier demodulation)	Multiple, to be determined by (1) symbol rate (2) S/N_0 at design point to preserve amplifier linearity
IF system linearity (i.e., allowance made for a 7-dB noise crest factor between RMS noise power and 1-dB signal gain compression)	$\frac{ST_{sy}}{N_0} = -1$ dB $(8.33 < R_{sy} < 220$ SPS) $\frac{ST_{sy}}{N_0} = -4$ dB $(220 < R_{sy} < 500$K SPS)
Gain stability at 10 MHz	Δ1 dB max. per 12 h and/or Δ5°C
Phase stability at 10 MHz	Δ5 deg max. per 12 h and/or Δ5°C
Input/output impedance	50-Ω nominal
Input signal level	−70 ±3 dBm
Baseband output level	Signal = ±140 mV, noise = ±5 V peak

[a]S = signal power; N_0 = noise density; T_{sy} = time period for 1 symbol; R_{sy} = symbol rate.

Table 2. Signal and noise profile

		Point 1 on Fig. 1		Point 2 on Fig. 1			Point 3 on Fig. 1		
Gain/bandwidth switch position	Symbol rate range, SPS	Signal	Noise	Signal	Noise[a]	Phase switch 1-dB gain compression	Signal	Noise[b]	Coherent amplitude detector 1-dB gain compression
1	8.33–100	−70	−7	−59	+4	+13	−17	+6	+13
2	100–1000	−70	−18	−58	+4	+13	−17	+5	+13
3	1000–4800	−70	−25	−41	+4	+13	−17	+5	+13
4	4800–22K	−70	−32	−34	+4	+13	−17	+4	+13
5	22K–100K	−70	−38	−28	+4	+13	−17	+5	+13
6	100K–500K	−70	−45	−23	+2	+13	−17	+5	+13

[a]Maximum noise bandwidth = 12 MHz.
[b]Noise power in the bandwidth associated with that symbol rate range.

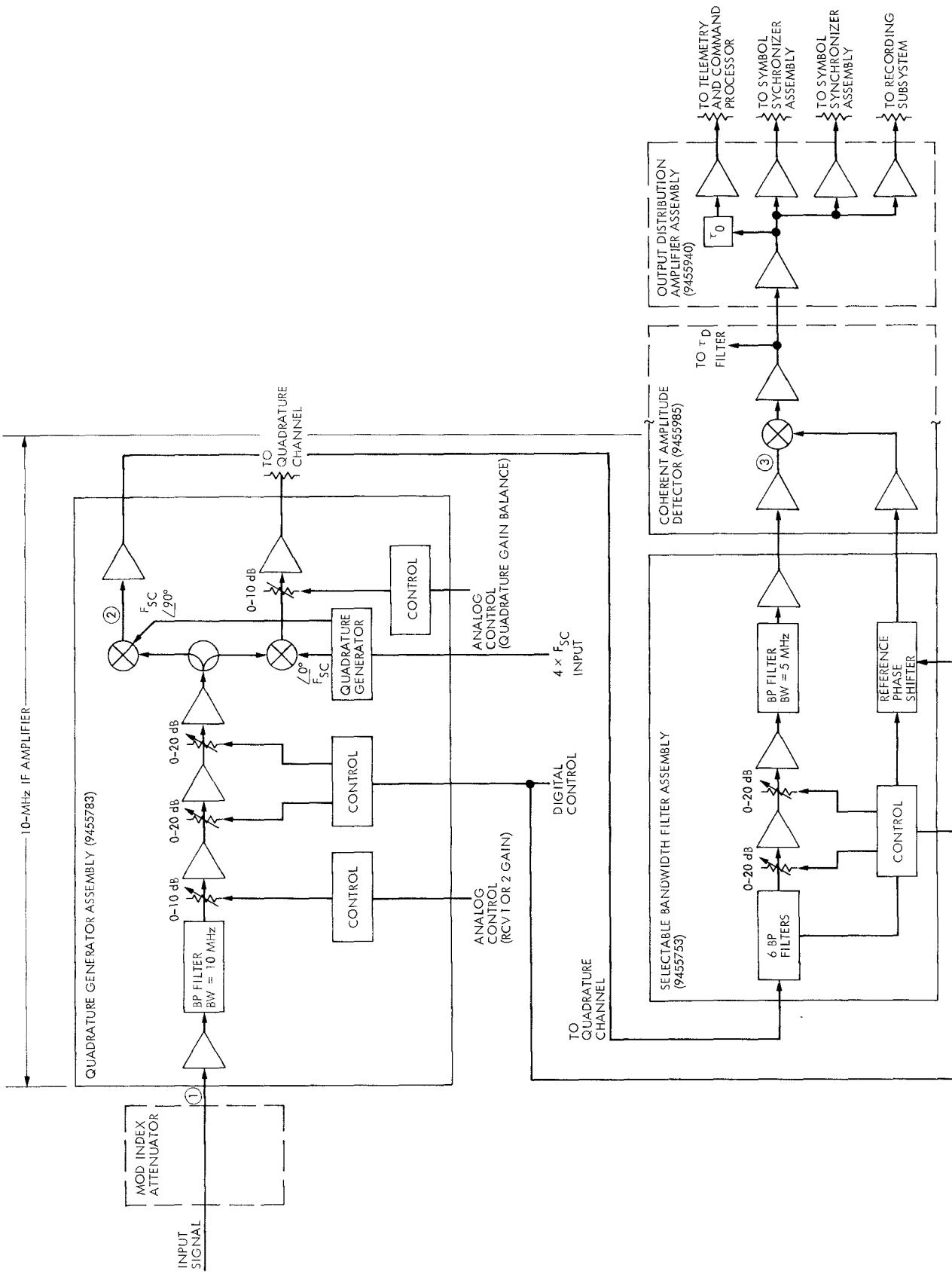

Fig. 1. Data channel block diagram

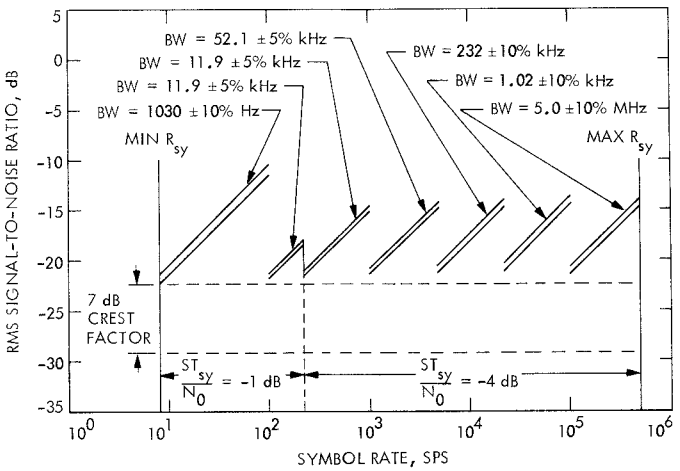

Fig. 2. Signal-to-noise ratio vs. symbol rate for six IF noise bandwidths